

WHAT IS CLAIMED IS:

- 1 1. A processor operable from an M-bit instruction set or an N-bit
2 instruction set, where M and N are integers, and M is less than N, comprising:
3 a memory unit for storing at least first and second instruction
4 streams respectively comprising N-bit instructions and M-bit instructions
5 an execution unit operable to receive execution signals to execute
6 the N-bit instructions;
7 a decode unit coupled to the memory unit and to the execution unit
8 to receive and decode the first and second instruction streams from the memory
9 unit to produce therefrom the execution signals, the decode unit including a
10 translation unit for receiving each of the M-bit instructions to translate each of a
11 first group of the M-bit instructions to a corresponding one of the N-bit
12 instructions, and to translate each of a second group of the M-bit instructions to
13 two or more N-bit instructions for decoding by the decode unit.
- 1 2. The processor of claim 1, wherein each of the M-bit and N-bit
2 instructions are stored in the memory unit at locations identified by memory
3 addresses having at least one bit position set to a first state to identify a memory
4 address of an M-bit instruction and a second state to identify a memory address
5 of an N-bit instruction.
- 1 3. The processor of claim 2, the N-bit instruction stream including
2 at least one N-bit branch instruction, the decode unit operating to execute the N-
3 bit branch instruction to switch from executing N-bit instructions to executing M-
4 bit instructions.
- 1 4. The processor of claim 1, where N is equal to 2M.
- 1 5. The processor of claim 1, wherein M is 16 and N is 32.
- 1 6. The processor of claim 2, wherein the one bit position is the
2 least significant bit of the memory address.
- 1 7. A processor unit, including
2 a memory for storing a plurality of instructions, including M-bit
3 instructions and N-bit instructions where M and N are integers and M is less than

4 N, each instruction being stored at a memory location identified by a memory
5 address, each memory address having a bit position set to a first state for M-bit
6 instructions and to a second state for N-bit instructions;

7 an instruction flow control unit for retrieving the instructions from the
8 memory for controlling execution of the retrieved instructions, the instruction flow
9 control unit including a translation unit operable to receive ones of the M-bit
10 instruction for translation to a sequence of two or more N-bit instructions.

1 8. A microprocessor, comprising:

2 a memory element containing a plurality of M-bit instructions and N-
3 bit instructions where M and N are integers and M is less than N;

4 an instruction fetch unit coupled to the memory element for
5 retrieving selected ones of the M-bit instructions or N-bit instructions therefrom,
6 the instruction fetch unit including,

7 a translator unit for translating each of the M-bit
8 instructions fetched from the memory element into a sequence of
9 one or more N-bit instructions; and

10 a decode unit coupled to the memory element and to
11 the translator unit for receiving each of N-bit instructions fetch from
12 the memory element and each of N-bit instructions from the
13 translator unit for decoding such N-bit instructions.

1 9. The microprocessor of claim 8, including at least one target
2 register for holding a target address, the plurality of N-bit instructions including a
3 prepare target instruction that, when executed by the microprocessor, loads the
4 target address in the target register.

1 10. The microprocessor of claim 9, wherein the plurality of N-bit
2 instructions includes a BLINK branch instruction operating to use the target
3 address in the target register to branch to cause an M-bit target instruction or an
4 N-bit target instruction to be fetched from the memory element for translation or
5 decode, respectively.

1 11. The microprocessor of claim 10, wherein the BLINK branch
2 instruction is an unconditional branch instruction.

1 12. The microprocessor of claim 9, wherein the target address
2 includes a bit position set to a first state to identify an M-bit target instruction.

1 13. The microprocessor of claim 12, wherein the bit position is set
2 to a second state to identify an N-bit target instruction.

1 14. A microcomputer formed on single chip, including
2 memory storing M-bit instructions and N-bit instructions where M
3 and N are integers, and N is greater than M;
4 a translator coupled to the memory to receive M-bit instructions for
5 translation of each received M-bit instruction to a sequence of one or more
6 N-bit instructions; and
7 a decoder coupled to the memory and to the decoder for receiving
8 and decoding the N-bit instructions.

1 15. The microcomputer of claim 14, wherein M is 16 and N is 32.

1 16. The microcomputer of claim 14, where the N-bit instructions
2 include an N-bit branch instruction that contains data indicative of a branch
3 address of a target instruction, the branch address having a bit position set to a
4 first state when the target instruction is an M-bit instruction.

1 17. A method of executing M-bit instructions and N-bit instructions
2 by a microcomputer formed on a single chip, M and N being integers, and
3 M is less than N, the method including the steps of:
4 storing the M-bit and N-bit instructions in a memory;
5 operating in a first mode to sequentially decode ones of the N-bit
6 instructions;
7 operating in a second mode to sequentially translate ones of the M-
8 bit instructions to a sequence of one or more N-bit instructions, and then
9 decoding the N-bit instructions.

1 18. The method of claim 17, wherein the N-bit instructions include
2 an N-bit branch instruction, and the step of operating in the first mode includes
3 decoding the N-bit branch instruction to branch to an M-bit instruction having a
4 memory address with a least significant bit set to a first state to switch from the
5 first state to the second state of operation.

1 19. In a microcomputer structured to execute N-bit instructions,
2 including an N-bit branch instruction, and M-bit instructions, including an M-bit
3 branch instruction, where M and N are integers, and N is greater than M, a
4 method of executing the M-bit instructions that includes the steps of:
5 emulating each of the M-bit branch instructions with a sequence of
6 one or more N-bit instructions;
7 emulating the M-bit branch instruction with a prepare to branch
8 instruction that provides a branch address and thereafter the N-bit branch
9 instruction that uses the branch address.

1 20. The method of claim 19, including the step of providing at least
2 one target address register, and the step of emulating the M-bit branch instruction
3 includes the prepare to branch instruction loading the target address register with
4 the target address.

1 21. The method of claim 20, the step of emulating the M-bit branch
2 instruction including the step of the N-bit branch instruction reading the target
3 address for the target address.

1 22. The microcomputer of claim 14, including a plurality of general
2 purpose registers each for storing data in response to one or more of the N-bit
3 instructions.

1 23. The microcomputer of claim 22, wherein the plurality of general
2 purpose registers each includes 2N bit positions.

1 24. The microcomputer of claim 22, wherein predetermined ones of
2 the one or more N-bit instructions load data in low-order bit positions of selected
3 ones of the plurality of general purpose registers.

1 25. The microcomputer of claim 22, wherein first ones of the one or
2 more N-bit instructions load data in low-order bit positions of selected one of the
3 plurality of general purpose registers, and second ones of the one or more N-bit
4 instructions load data in high-order bit positions of the plurality of general purpose
5 registers.

1 26. The microcomputer of claim 22, wherein predetermined ones of
2 the one or more N-bit instructions load data in low-order bit positions of selected
3 ones of the plurality of general purpose registers with extension of the most
4 significant bit of the data replicated in high-order bit positions of the selected ones
5 of the plurality of general purpose registers.